REMARKS

The application includes claims 1-19 prior to entering this amendment.

The examiner objects to claims 3 and 19 for informalities.

The examiner finds claims 2-8 and 10-13 allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The examiner rejects claims 1, 9, and 14-19 under 35 U.S.C. § 103(a) as being unpatentable over Zheng (U.S. patent application publication 2004/002323) in view of DeWulf (U.S. patent 6,590,528), Ishizuka et al. (U.S. patent 4,531,089), and Kingsbury et al. (U.S. patent 6,308,155).

The applicants amend claims 2-3 and 10, cancel claims 1, 9, and 14-19, and add claims 20-29.

The application remains with claims 2-8, 10-13, and 20-29 after entering this amendment.

The applicants add no new matter and request reconsideration.

Claim Objections

The applicants amend claim 3 to reflect it depends from claim 2 and cancel claim 19 to thereby obviate the examiner's objections to claims 3 and 19.

Claims Allowable

The applicants amend claims 2 and 10 in independent form including all of the limitations of the corresponding base and any intervening claims. Claims 2-8 and 10-13 are in condition for the examiner's allowance.

Claim Rejections Under § 103

The examiner rejects claims 1, 9, and 14-19 as obvious over Zheng in view of DeWulf, Ishizuka, and Kingsbury. The applicants disagree for the reasons that follow.

The present application describes embodiments of staggered Automatic Gain Control (AGC) with a digitally controlled Variable Gain Amplifier (VGA) that overcomes phase or gain imbalances associated with existing circuits by providing staggered AGCs each associated with respective I and Q digitally controlled VGAs. The control of the AGCs is done locally to the AGCs rather than globally from a DSP function in the digital portion of the receiver.

Claim 20 recites *a detector to generate a detect signal by detecting a difference between the I and Q signals.* Claim 25 recites *generating a detect signal by detecting a difference between I and Q signals at respective outputs of I and Q variable gain amplifiers of a plurality of serially connected automatic gain control stages.* The examiner acknowledges that Zheng does not disclose "locally generated control signals using detection and digitizing."[1] The examiner alleges, however, that Ishizuka fills the gap with its elements 3, 5-7, and 11. Ishizuka, however, does not disclose a detector that generates a detect signal by detecting a difference between I and Q signals as required by the claim. Rather, Ishizuka's gain setting circuit 5 generates the gain control signal on the basis of the power calculated by the power calculating circuit 11. That is, the circuit 11 calculates the power of the signal at the output of the A/D 7 (at terminal 2), but does not detect differences between I and Q signals as would be necessary to obviate claims 20 and 25.

Claim 20 recites *an ADC to convert the detect signal to a digital detect signal.* Claim 25 recites *converting the detect signal to a digital detect signal.* Even if Ishuzuka's A/D 7 is placed prior to detection, as the examiner suggests,[2] the A/D 7 does not convert a detect signal that indicates a difference between the I and Q signals, as it must to obviate the claims.

Claim 20 recites *an engine to generate a local control signal responsive to the digital detect signal* and *where the I and Q VGAs operate responsive to the local control signal.* Claim 25 includes similar limitations. Although not entirely clear, the examiner appears to allege that Zheng's gain mismatch estimator 40 discloses the recited engine. But the gain mismatch estimator 40 does not generate a control signal responsive to the digital detect signal, where the detect signal indicates a difference between I and Q paths. Rather, the gain mismatch estimator 40 automatically determines the orientation of the adjusting based on calculating the correlation value, in turn, determined from signals output from the correlator 30, in turn, determined from signals out from the complex filter signal extractor 20, and combining blocks 60a and 60b. In short, Zheng's mismatch estimator 40 does not generate the α and β signals that control the VGAs 51a and 51b responsive to differences between signals I and Q, rather the mismatch estimator 40 operates as follows.

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[1] Office action dated 11/14/2006, page 3.
[2] Id.

"A gain mismatch estimator is used to decide automatically the orientation of the adjusting (adding or reducing) of the gains α and β. To implement this, the adjusting of the value of α or β in current time will be determined by both the changed values of α or β in the last time and the changed value of $C_r(t)$ in the last time, see FIG. 1. The adjusting of gain should be in a way, which will force $C_r(t)$ to continuously decrease. After the compensation by the compensator, the mismatch between signal $S_{CI}(t)$ and $S_{CQ}(t)$ will be greatly reduced no matter how large a mismatch exists between $S_I(t)$ and $S_Q(t)$, and thus the IRR will be significantly improved."[3]

Conclusion

For the above reasons, the applicants request reconsideration and allowance of the remaining claims. Please telephone the undersigned at (503) 222-3613 if it appears that an interview would be helpful in advancing the case.

Respectfully submitted,

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[3] Ishizuka, paragraph 0030.